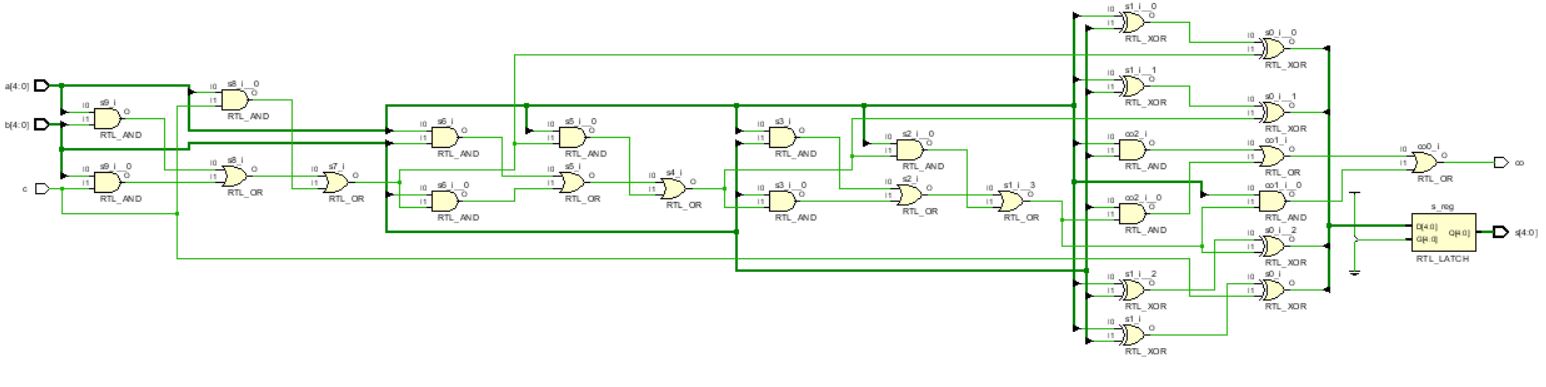
**Practical 7**

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|  |

**RTL DIAGRAM: **

**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_adder\_16b\_bh is

generic(N : integer:=15);

-- Port ( );

end Tb\_adder\_16b\_bh;

architecture Behavioral of Tb\_adder\_16b\_bh is

component adder\_16b\_bh is

Port ( a : in STD\_LOGIC\_VECTOR (N downto 0);

b : in STD\_LOGIC\_VECTOR (N downto 0);

c : in STD\_LOGIC;

s : out STD\_LOGIC\_VECTOR (N downto 0);

co : out STD\_LOGIC);

end component adder\_16b\_bh;

signal a1 : STD\_LOGIC\_VECTOR (N downto 0);

signal b1 : STD\_LOGIC\_VECTOR (N downto 0);

signal c1 : STD\_LOGIC;

signal s1 : STD\_LOGIC\_VECTOR (N downto 0);

signal c01 : STD\_LOGIC;

begin

X1:adder\_16b\_bh port map(a1,b1,c1,s1,c01);

process

begin

c1<='0';

a1<="0000000000000000";

b1<="0000000000000000";

wait for 10ns;

a1<="1111111111111111";

b1<="0000000000000000";

wait for 10ns;

a1<="1111111111111111";

b1<="1111111111111111";

wait for 10ns;

a1<="1111111111111111";

b1<="1010101010101010";

wait for 10ns;

c1<='1';

a1<="0000000000000000";

b1<="0000000000000000";

wait for 10ns;

a1<="1111111111111111";

b1<="0000000000000000";

wait for 10ns;

a1<="1111111111111111";

b1<="1111111111111111";

wait for 10ns;

a1<="1111111111111111";

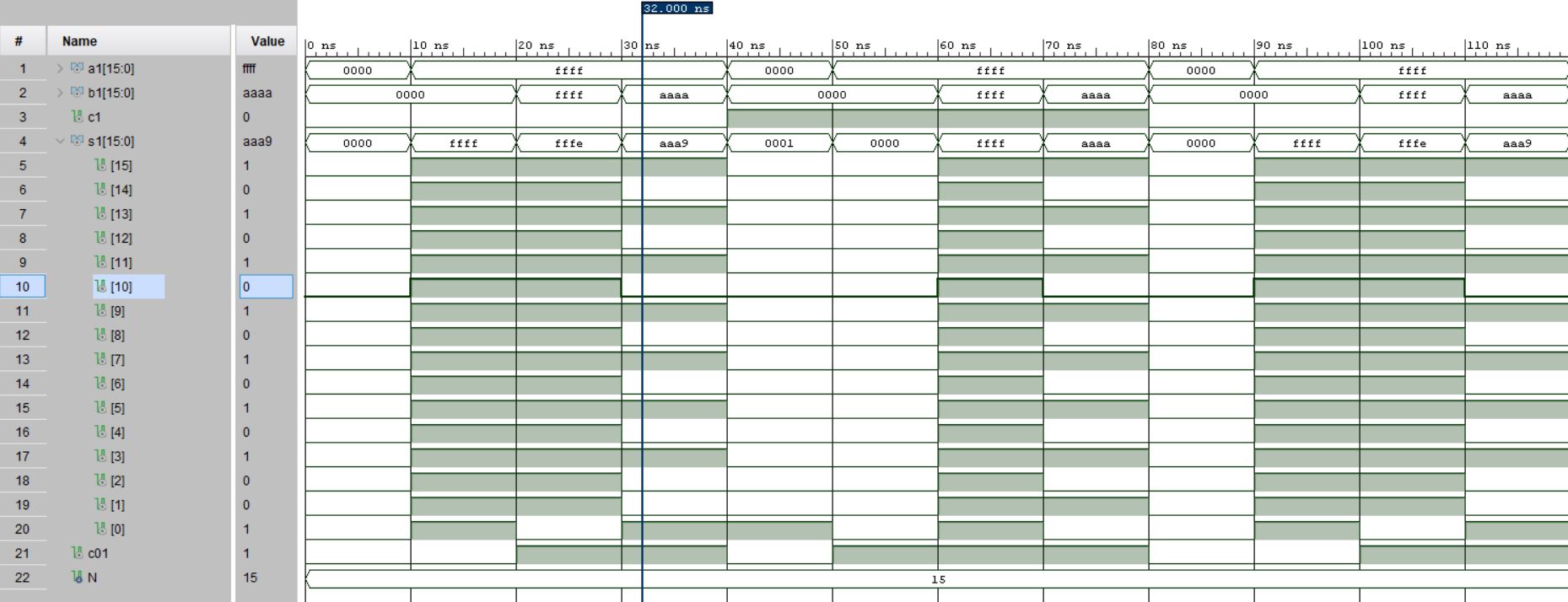
b1<="1010101010101010";

wait for 10ns;

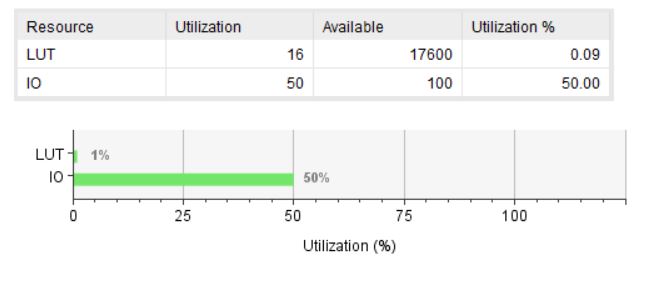
end process;

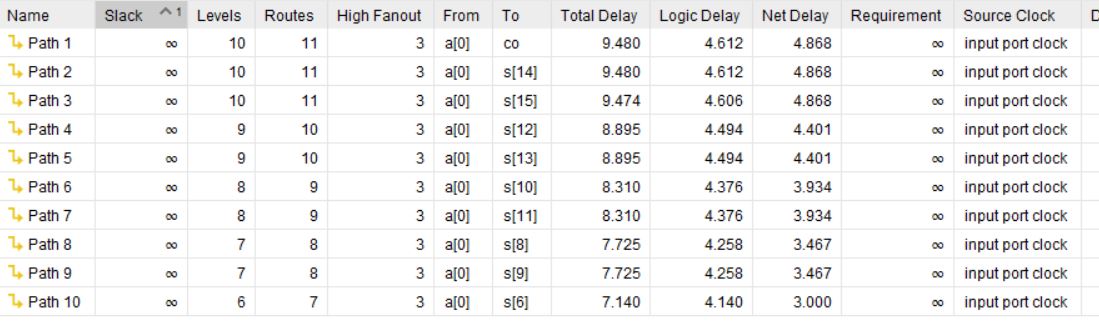
end Behavioral;

**SIMULATION WAVEFORM :**

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**SYNTHESIS SUMMARY:**

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Maximum Combinational Delay: 9.480nSec